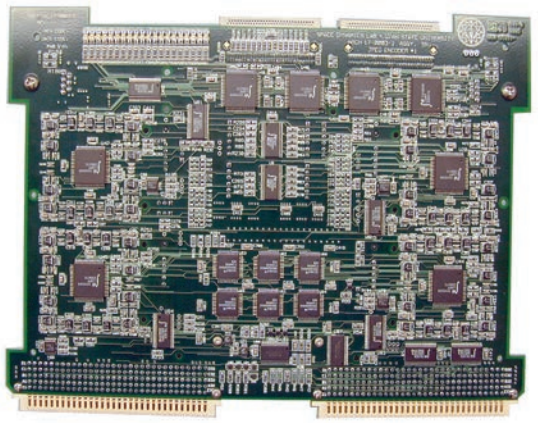
SDL/00-031 D

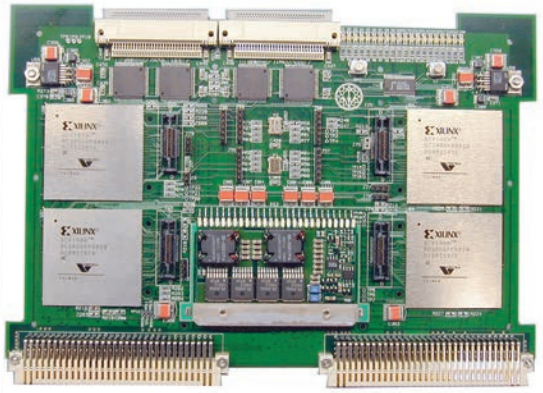
ARCH

Advanced Reconnaissance Compression Hardware

The Space Dynamics Laboratory has developed the ARCH state-of-the-art imagery compression technology for use in next-generation reconnaissance pod systems. This system-configurable hardware set is designed to operate in the harsh TAC/RECCE environment and uses Commercial Off-The-Shelf (COTS) hardware to provide real-time compression for many EO/IR sensor types (e.g., large format framing and scanning sensors). The ARCH JPEG compression format meets the latest NITFS requirements for TAC/RECCE imagery. ARCH accepts a maximum input data rate of 160 Mpixels/second.



The ARCH compression system consists of a set of five formatting, compression, and interface boards: an input formatter board with camera interface, two JPEG compression boards, an output formatter board with NITF interface, and an output data controller board with CDL and Digital Storage System (DSS) interfaces. The ARCH receives image and NITF header data from an EO/IR sensor. The input formatter receives the image data, while the NITF data are sent directly to the output formatter. The input formatter divides the image data and passes it to the two encoder cards in parallel for processing by the JPEG algorithm. The output formatter combines the encoded JPEG images with the supplied NITF data, updates NITF fields where necessary, and generates a single output image file. This compressed output file is then passed to a real-time data link (CDL) and/or storage device (DSS).



SPECIFICATIONS

- Five-card encoder set provides real-time image compression:
  - 8 or 12 bit imagery
  - Programmable rate and image size, including:
    - 2k x 2k pixels/frame at 30 frames/second
    - 5k x 5k pixels/frame at 4 frames/second
    - 10k x 10k pixels/frame at 1.25 frames/second
    - 12k pixels/scan at 2500 scans/second
    - 5k pixels/scan at 5000 scans/second
- Meets the National Imagery Transmission Format Standard (NITFS):
  - NITFS version 2.1
  - Joint Photographic Experts Group (JPEG) format
- Multiple interfaces, including:
  - Electro-optical/infrared (EO/IR) camera
  - Solid State or digital tape recorder
  - Common Data Link (CDL)
- Single-band or dual-band band mode
- Built-In Test (BIT) capability
- Common VME-64 interface
- Programmable compression tables
- Modular design will accommodate future higher rate single- and multi-band sensors

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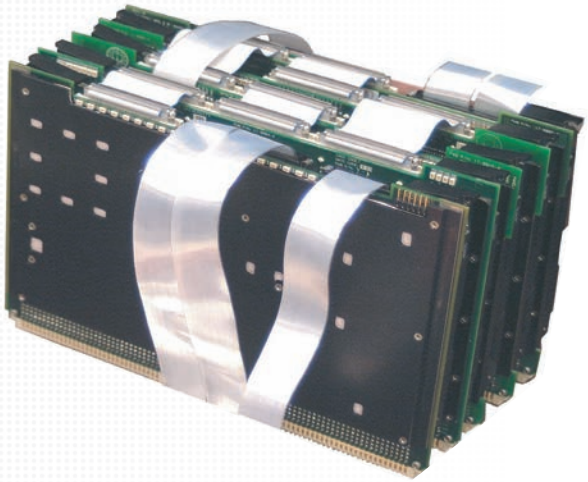
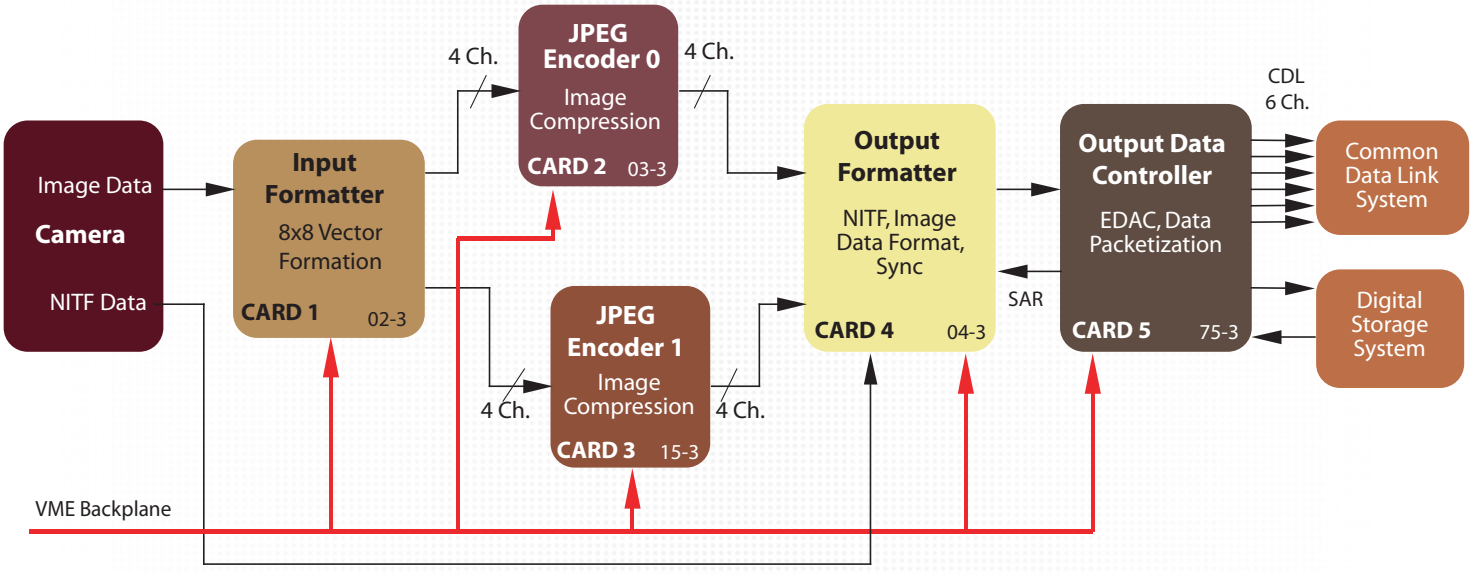
ARCH FEATURES



The ARCH suite will accept data from external EO/IR sources up to a peak data rate of 320 Mbytes per second and compress, format, and transmit the resulting data to a real-time data link and/or digital storage system with latency no greater than five seconds. Data is processed by ARCH in accordance with NITF standards for data compression and formatting of TAC/RECCE imagery. ARCH can support the processing of single image frames of up to 12,288 x 12,288, currently processing EO data at 8 bits/pixel and IR data at 12 bits/pixel. Compression and integrity of the image data is controlled by the user through the selection of a quantization table and the enable/disable of an error detection and correction encoding system.

The five ARCH cards reside in a custom chassis that conforms to the dimensional requirements of a short Aircraft Transport Rack (ATR) enclosure. ARCH utilizes conduction-cooled VME cards that interface with the 6U VME 64 backplane of the chassis as well as direct input/output interfaces with the sensor, CDL, and digital storage system. The backplane also supplies the necessary 50 watts of power to the suite. A VME-enabled processor residing in the ATR provides the user with a software command and status interface for the ARCH suite.

The ARCH input formatter card receives uncompressed image data directly from the sensor via a Low Voltage Differential Signaling (LVDS) interface at an input rate of up to 160 Mpixels/second. The data is formatted into eight sub-images divided along the horizontal dimension, which are then passed to the encoder cards for processing. The two encoder cards encode the sub-images in parallel using four hardware-based JPEG compression engines per card. The resultant eight individual JPEG files are passed to the output formatter for recombination. The output formatter also receives the corresponding NITF data from the sensor via an LVDS interface, modifies it appropriately, and builds a complete NITF image product suitable for TAC/RECCE exploitation. The NITF file is then sent to the output data controller card where error detection and correction functions are performed and the data is packetized for CDL transfer. Data is transferred out of the output data controller to either the digital storage system via a DCRsi-type interface or the CDL via ECL signals at rates up to 320 Mbits/second. The output data controller can also read back data from the digital storage system and transmit over the CDL link at rates up to 257 Mbits/second.



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